

REMARKS

Applicant hereby adds claims 81-82. Accordingly, claims 21-30 and 61-82 are pending in the present application.

Claims 61-62 and 71-72 stand rejected under 35 USC 112, first paragraph. Claims 21-30, 69-70, and 79-80 stand rejected under 35 USC 102 for anticipation by U.S. Patent No 5,960,276 to Liaw et al.

Applicant respectfully traverses the rejection and urges allowance of the present application.

Referring to the alleged constructive election and in the event that the application is not allowed, Applicants respectfully traverse the election/restriction and allegation that Applicants have constructively elected any claims and request examination of such properly pending claims. 37 CFR 1.145 states that restriction is proper if the applicant presents claims directed to an invention distinct from and independent of the invention previously claimed. Applicants added new *dependent* claims 61-80 by amendment. The dependent claims *depend from and recite further limitations* in addition to those recited in independent claims 21 or 26. Accordingly, the recitation of additional limitations in the dependent claims further defines the invention defined by the respective independent claims 21 or 26 and such *further definition in the dependent claims can not be considered "distinct from and independent of" the invention* defined by the independent claims as required for a proper restriction. By definition, the newly added dependent claims are not distinct from and independent of the previously pending claims from which they depend. If restriction/election is still deemed proper (although improper for the reasons stated herein) Applicants request the opportunity to

elect the claims pursuant to MPEP 821.03 and 37 CFR 1.145 which both provide that "applicant will be required to restrict the claims" (emphasis added).

For a proper anticipation rejection, MPEP 2131 provides a claim is anticipated only if each and every element as set forth in the claim is found, either expressly or inherently described, in a single prior art reference. *Verdegaal Bros. v. Union Oil Co. of California*, 814 F.2d 628, 631, 2 USPQ2d 1051, 1053 (Fed. Cir. 1987). In addition, the claim elements must be arranged as required by the claim for a proper anticipation rejection. *In re Bond*, 910 F.2d 831, 15 USPQ2d 1566 (Fed. Cir. 1990).

Referring to claim 21, the teachings of col. 4, lines 55-65 are identified as allegedly disclosing the *one series of transistors being formed to have active area widths less than one micron to achieve lower threshold voltages than the other of the series of transistors*. The identified teachings fail to teach limitations of claim 21. More specifically, the teachings are devoid of any reference to threshold voltages as related to dimensions of the series of transistors. Liaw describes the relationship of channel widths and lengths with respect to threshold voltage in the Table in col. 4. As established by Fig. 3B, channel width 42 refers to the y axis direction and channel length L refers to the x axis direction. Referring to the chart, for a given channel width (e.g., 20 of the table), first active areas having dimensions (e.g., L=20) greater than second active areas (e.g., L=0.35) have smaller respective threshold voltages (e.g., $0.643 < 0.685$). Accordingly, the teachings of Liaw are directly opposite to the limitations of claim 1 wherein larger x direction dimensions of Liaw (Fig. 3B) are disclosed as having smaller threshold voltages compared with devices having smaller x direction dimensions. The limitations of claim 1 including the other series having active

area widths greater than one micron and the one series being formed to have active area widths less than one micron to achieve lower threshold voltages than the other of the series are not shown nor suggested by the prior art and claim 1 is allowable for at least this reason.

The teachings relied upon by the Office fail to disclose or suggest arrangement of the claim elements as required by the claim for a proper anticipation rejection and accordingly are deficient with respect to the alleged anticipation rejection. In particular, 37 C.F.R. §1.104(c)(2) provides that *the pertinence of each reference, if not apparent, must be clearly explained and each rejected claim specified*. Further, 37 C.F.R. §1.104(c)(2) states that the Examiner must cite the best references at their command. When a reference is complex or shows or describes inventions other than that claimed by Applicants, the particular teachings relied upon must be designated as nearly as practicable. The pertinence of each reference if not apparent must be clearly explained for each rejected claim specified. Applicants respectfully request clarification of the rejections with respect to specific references and specific references teachings therein pursuant to 37 C.F.R. §1.104(c)(2) in a non-final Action if any claims including claim 1 are not found to be allowable.

In addition, the Office appears to misinterpret the teachings of Liaw and Applicants respectfully request issuance of a non-Final action to clarify inconsistencies in the Action if claim 21 is not allowed. In particular, NMOS and PMOS teachings 13 and 15 are identified on page 3 of the Action and apparently relied upon as disclosing the two series of field effect transistors defined in claim 1. However, the teachings 12W and 12N identified on page 3 as allegedly disclosing active area widths greater than and

less than 1 micron refer only to NMOS devices. If claim 21 is not allowed, Applicants respectfully request clarification of the rejection of claim 21 in a non-Final Action and specific identification of the reference teachings relied upon as disclosing the two series of FETs as well as the active area widths and respective threshold voltages in accordance with 37 C.F.R §1.104(c)(2).

The claims which depend from independent claim 21 are in condition for allowance for the reasons discussed above with respect to the independent claim as well as for their own respective features which are neither shown nor suggested by the cited art.

Referring to claim 22, the Office relies upon the teachings of NMOS and PMOS as allegedly disclosing the threshold voltages for the two series of FETs are defined by a common channel implant. However, the dimensions of Liaw are only discussed relative to NMOS devices. In addition, the PMOS areas 15 are covered by a photoresist layer prior to any implanting of Boron as disclosed by col. 3, lines 30-35 contrary to the statements set forth in the Action. Further, the teachings identified in the Action (col. 3, lines 30-45) are void of any teaching or suggestion relative to threshold voltages. Pursuant to the CFR, Applicant respectfully requests clarification of any rejection of claim 22 in a *non-final* Action if claim 22 is not allowed so Applicant may properly respond during the prosecution of this application.

Referring to claim 23, the identified teachings refer to advantages of embodiments utilizing the invention of Liaw compared with prior art devices and fail to provide any teachings related to a common channel implant defining the threshold voltages for the two series of FETs and being the only channel implant which defines

the threshold voltages as claimed. Limitations of claim 23 are not disclosed nor suggested by the art and claim 23 is allowable for at least this reason. Pursuant to the CFR, Applicant respectfully requests clarification of any rejection of claim 23 in a *non-final Action* if claim 23 is not allowed so Applicant may properly respond during the prosecution of this application.

Referring to claims 24-25, Liaw is void of any teaching or suggestion of implanting the PMOS regions with boron to define the threshold voltages as alleged by the Office in support of the rejection of claims 24-25. Limitations of claims 24-25 are not disclosed nor suggested by the art and claims 24-25 are allowable for at least this reason. Pursuant to the CFR, Applicant respectfully requests clarification of any rejection of claims 24-25 in a *non-final Action* if claims 24-25 are not allowed so Applicant may properly respond during the prosecution of this application.

Referring to claim 30, Boron is not implanted into the PMOS regions to define the threshold voltages as clearly set forth by the teachings of col. 3 of Liaw. Pursuant to the CFR, Applicant respectfully requests clarification of any rejection of claim 30 in a *non-final Action* if claim 30 is not allowed so Applicant may properly respond during the prosecution of this application. Applicants request identification of the specific reference teachings relied upon as disclosing the claimed two series of FETs and the common channel implant comprising the only channel implant to define the threshold voltages for the two series of FETs.

Referring to claim 26, the Office recites the Table as allegedly disclosing achieving different threshold voltages between transistors in different series by varying the active area widths of the transistors in the series. The table fails to disclose

transistors having active areas widths less than active areas of other transistors have threshold voltages less than the threshold voltages of the other transistors. In one example and as established by Fig. 3B, channel width 42 refers to the y axis direction and channel length L refers to the x axis direction. Referring to the chart, for a given channel width (e.g., 20 of the table), first active areas having dimensions (e.g., L=20) greater than second active areas (e.g., L=0.35) have smaller threshold voltages (e.g., $0.643 < 0.685$). Limitations of claim 26 are not shown nor suggested by the prior art and claim 26 is allowable for at least this reason.

The claims which depend from independent claim 26 are in condition for allowance for the reasons discussed above with respect to the independent claim as well as for their own respective features which are neither shown nor suggested by the cited art.

Referring to the rejections under 35 USC 112, first paragraph, Applicants respectfully refer the examiner to the teachings of Figs. 3-4 and the associated specification teachings as disclosing and describing the transistors of the two series as having a single geometry type. The Examiner is respectfully reminded that MPEP §2163.02 (8th Edition) states the test for sufficiency of support in an application is whether the disclosure relied upon "reasonably conveys to the artisan that the inventor had possession at that time of the later claimed subject matter." MPEP §2163.02 (8th Edition) citing *Ralston Purina Co. v Far-Mar-Co., Inc.*, 772 F.2d 1570, 1575, 227 USPQ 177, 179 (Fed. Cir. 1985). Notably, the subject matter of the claim need not be described literally (i.e., **using the same terms** or *in haec verba*) in order for the disclosure to satisfy the description requirement. MPEP §2163.02 (8th Edition). In the

instant case, the specification recitation and figures are clearly directed towards transistors in the disclosed embodiments of Figs. 3-4 having a common geometry type (e.g., planar in one embodiment), as opposed to plural series of different types - one stacked and one trench or other arrangements of different geometry types of transistors. The limitations of claims 61-62 and 71-72 are clearly supported and described by the originally-filed application and Applicant requests withdrawal of the 112, first paragraph in the next Action.


Applicants hereby add new claims 81-82 which are supported at least by Figs. 2-3 and associated specification teachings of the originally-filed application.

The Examiner is requested to phone the undersigned if the Examiner believes such would facilitate prosecution of the present application. The undersigned is available for telephone consultation at any time during normal business hours (Pacific Time Zone).

Respectfully submitted,

10/4/04

Date



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